An FPGA-based Sound Field Renderer for High-Precision Sound Field Auralization

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(i) Introduction

- Sound field auralization is **computation-intensive and memory-intensive**. The solutions include FPGA-based direct hardware implementation and software simulations on general-purpose processors and GPU[1].
- Accurate room impulse response is critical to achieve precise auralization results. The wave-based methods provide high accuracy, but require much higher computational capability since spatial grids are oversampled to suppress dispersion errors. In this research, **an FPGA-based accelerator** is developed to speed up computation in the generation of room impulse response through a sound field renderer.

(ii) System Design and Implementation

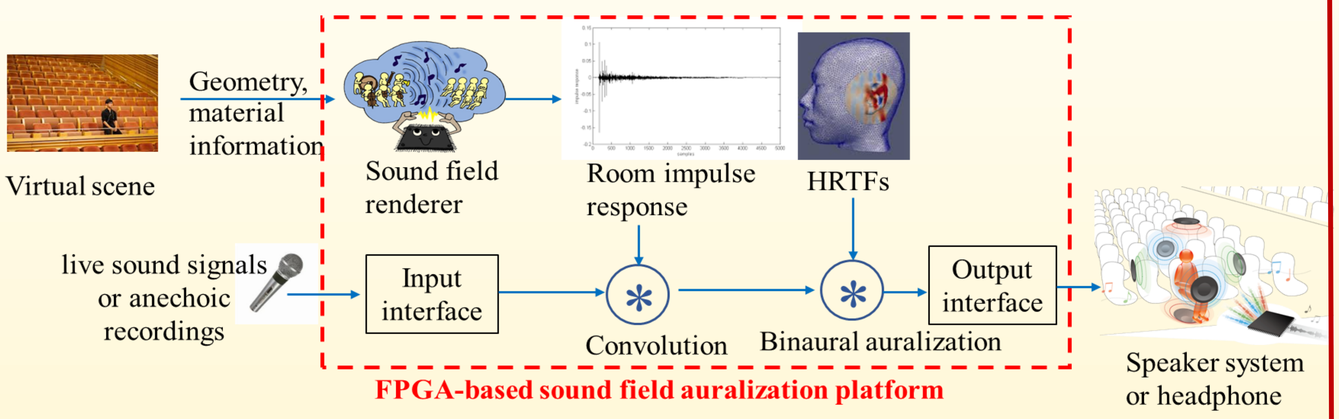
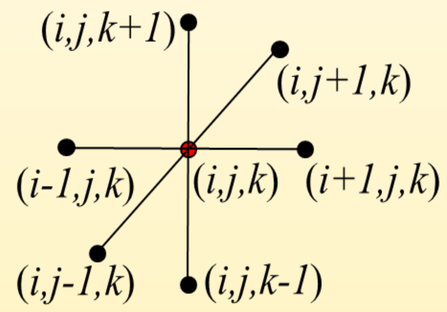


Fig. 1 Sound field auralization system

Rendering Algorithm

$$\frac{\partial^2 P}{\partial t^2} = c^2\left(\frac{\partial^2 P}{\partial x^2} + \frac{\partial^2 P}{\partial y^2} + \frac{\partial^2 P}{\partial z^2}\right)$$

Second-order central difference method in time domain



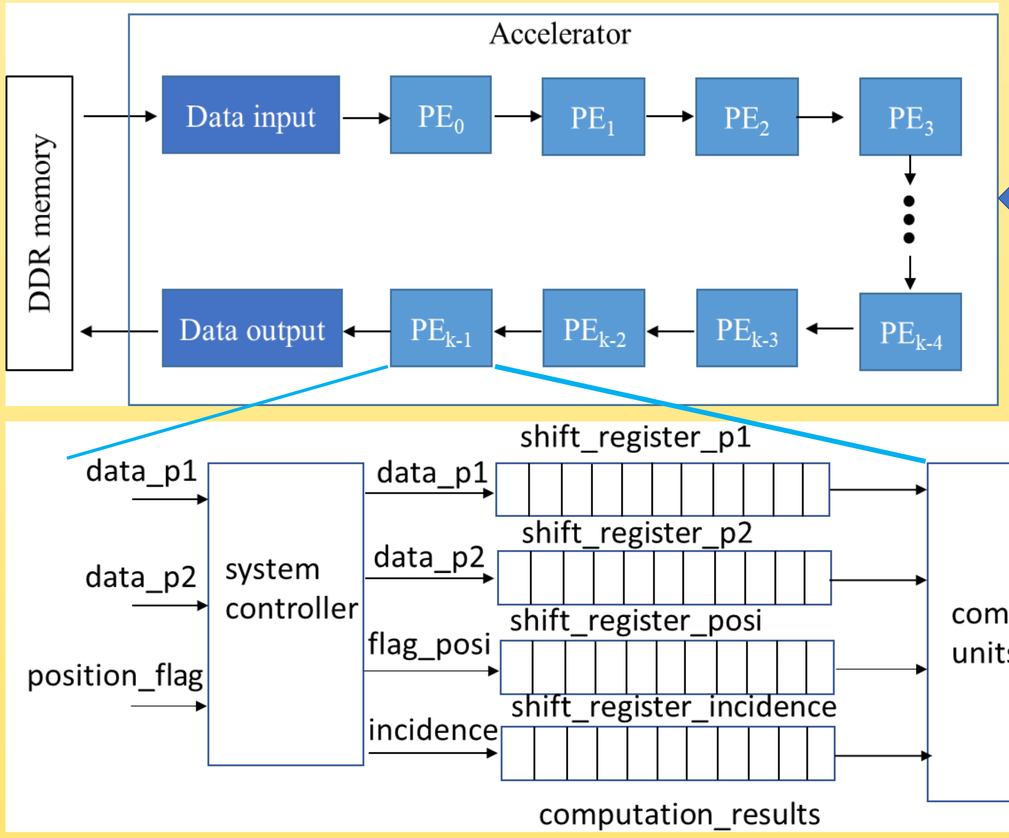
$$P^n(i,j,k) = D1 \times \left[P^{n-1}(i-1,j,k) + P^{n-1}(i+1,j,k) + P^{n-1}(i,j-1,k) + P^{n-1}(i,j+1,k) + P^{n-1}(i,j,k-1) + P^{n-1}(i,j,k+1) + 2P^{n-1}(i,j,k)\right] - D2 \times P^{n-2}(i,j,k)$$

Table 1: *Parameters*

Grid Position	D1	D2
General	1/4	1
Interior	$\frac{R+1}{2\,(R+3)}$	$\frac{3R+1}{R+3}$
Edge	$\frac{R+1}{8}$	R
Corner	$\frac{R+1}{2\,(5-R)}$	$\frac{5R-1}{5-R}$

- The explicit compact FDTD rendering algorithm is applied to compute room impulse response, and 7-point stencil scheme is adopted.
- D1 and D2 are based on reflective boundary conditions. They are chosen according to the position of grids.
- To update sound pressure of a grid requires six additions, one subtraction, one shift operation, and two multiplications.

System Design



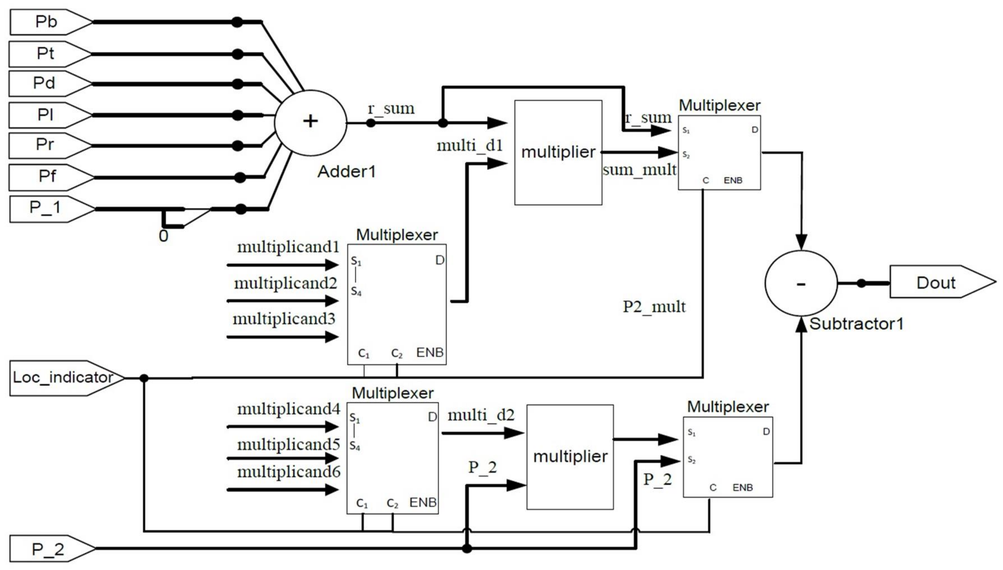


Figure 3. Computing unit.

System Implementation

- System is designed using OpenCL and implemented by using a DE10-Pro FPGA card. **Spatial and temporal blockings** are applied to alleviate the required external memory bandwidth and reuse data, respectively.
- The sound field renderer consists of the Data input module, computation engine, and the Data output module. The computation engine contains 16 PEs (processing elements) to compute sound pressures of grids in a spatial block at continuous 16 time-steps.
- **High-speed and high-bandwidth on-chip memories** is employed to implement a sliding-window-based data buffering to reduce the required memory bandwidth and data access overhead between the rendering engine and on-board external memory.

(iii) Performance Evaluation

Evaluation environment

	FPGA	Software Simulation
Computing unit	Stratix 10 SX (1SX280HU2F50E1VG)	Intel Xeon Gold 6212U
Cores	5760 DSP blocks	24 cores
Clock frequency	357 MHz	2.4 GHz
External memory	8 GB DDR4-2400	512 GB DDR4-2933
OS	CentOS 7.2	CentOS 7.2
Programming language	OpenCL	C
Compiler	Intel FPGA SDK for OpenCL 19.1	gcc 4.8.5

- **Sound space: 16m×8m×8m; Time steps: 32 ; Block size: 128 x 128**
  Data: single precision floating points; # of PEs: 16

Hardware resource utilization

Table 1: Hardware resource utilization

Logic utilization	DSP blocks	RAM blocks	Clock frequency
269,159 (29%)	342 (6%)	1785 (15%)	357 MHz

Rendering time

Table 2 Rendering Time Per Time Step (s)

FPGA	Software Simulation
0.0486	0.5363

(iv) Acknowledgements

Thanks for Intel's donation of the FPGA board DE10-Pro and the software tools through University Program. This work was supported by the JSPS KAKENHI Grant Number JP19K12092 and JP22K12123.

Reference:

[1] Y. Tan, T. Imamura, and M. Kondo, "FPGA-based acceleration of FDTD sound field rendering", Journal of the Audio Engineering Society, Vol. 69, No. 7/8, pp. 542-556, 2021.