Ultrasonic Wavefront Computing for Fourier Analysis

K.T.C. Chai*[1], D. Chen[1], J.C.E. Png[2], V.P. Bui[2], M.H. Dao[2], M.M.S. Sabry Aly[3] and A. Lal[4]
[1]Institute of Microelectronics, A*STAR, Singapore; [2]Institute of High Performance Computing, A*STAR, Singapore;
[3]Nanyang Technology University, Singapore; [4]Cornell University, NY, USA; chaitc@ime.a-star.edu.sg

1 Introduction

Fourier transform (FT) is a ubiquitous tool found in engineering and science. Variants like the Fast Fourier transform (FFT) can be computed with multicores [1], graphic processors [2], digital signal processors, etc., but these computing hardware become inefficient for arbitrary large dataset. An optical processor [3] which uses optics to produce FT naturally is comparatively more efficient. However, it is unable to resolve complex amplitude due to the difficulty in phase measurement with typical camera sensors. The acoustic method (ultrasound) which also operates by the principles of wave mechanics can be operated at compatible CMOS frequencies (GHz) [4] to acquire the phase information required for complex FT.

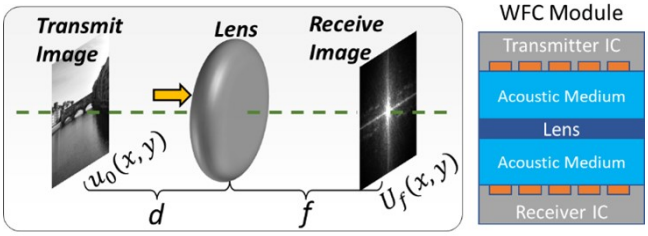

Figure 1: Illustration of the wavefront computing concept.

1.1 Wavefront Computing (WFC)

From Figure 1, the transmitter IC takes an input and generates a modulated GHz ultrasonic wave with precise spatial amplitude and phase information. These waves propagate as k-vectors across the acoustic stack and are summed / received by the receiver IC at the focal plane f as the FT. The speed of FT computation is determined by the propagation delay of the ultrasonic waves.

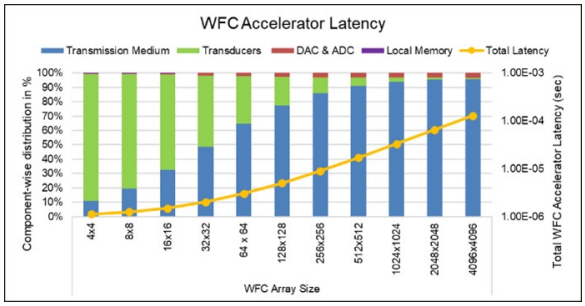

Figure 2: Contributions to latency in a WFC module.

2 Compact Modelling of WFC

A compact model [5] of the WFC module was developed with latency and power included as criteria for performance evaluation. The components of the model are wave transmission medium, transducer (low-noise receiver), drivers (DAC), analog-to-digital converters (ADC) and local memory. Figure 2 and 3 shows contributions breakdown for different-sized WFC arrays. The DAC, ADC and local memory perform signal processing and their impact on power as shown reduces for larger arrays due to resource sharing. For larger arrays, the transmission medium dominates latency while transducers dominate power due to the aggregative nature of array scaling.

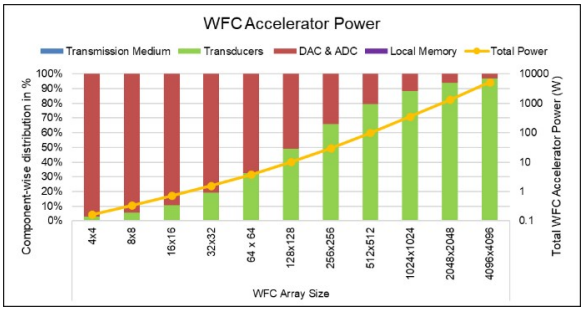

Figure 3: Contribution to power in a WFC module.

3 Evaluation of WFC for FT

For practical applications, we used $2D$ data sets $N \times N$ as input and generated the equivalent FT with different WFC module sizes $\delta \times \delta$. Direct mapping was used if dataset $\leq$ WFC array, while recursive decimation based on Cooley–Tukey algorithm was used when dataset > WFC array. The Energy Delay Product (EDP) (latency × power) metric was used in our evaluation to compare against the baseline multicore processor in [5] and the results are shown in Table 1. It is evident that our WFC module performs better as the dataset becomes larger. By nature, WFC processes data in parallel as opposed to needing radix decimation like digital electronic processors, hence, is more efficiently thru higher speed and lower power overhead. A prototype WFC module has been built and will be evaluated against our compact model.

Table 1: EDP Gain Evaluation against baseline

WFC Config. $\delta \times \delta \rightarrow$	$N \times N$	$\frac{N}{2} \times \frac{N}{2}$	$\frac{N}{4} \times \frac{N}{4}$	$\frac{N}{8} \times \frac{N}{8}$	$\frac{N}{16} \times \frac{N}{16}$
Data $\downarrow$	Energy Delay Product Gain:				
64×64	1.10	1.08	1.03	0.90	0.59
128×128	1.37	1.33	1.26	1.07	0.69
256×256	2.49	2.31	2.09	1.69	1.04
512×512	10.02	7.99	6.48	4.68	2.71
1024×1024	97.69	51.95	33.85	20.55	11.34
2048×2048	761.08	207.91	109.3	58.20	32.60
4096×4096	2317.3	366.53	185.5	97.08	57.06

4 Acknowledgments

Sponsored by A*STAR RIE2020 AME Prog. Fund A19E8b0102.

References

[1] F. Franchetti et al., *https://doi.org/10.1109/MSP.2009.934155*
[2] N. K. Govindaraju et al., *https://doi.org/10.1109/SC.2008.5213922*
[3] S. Perrin et al., *arXiv:1802.07161*
[4] Y. Liu et al., *https://doi.org/10.1109/ULTSYM.2018.8579938*
[5] D. A. Patel et al., *https://doi.org/10.1109/ASP-DAC52403.2022.9712586*