2.5D Photonic Interposer for High-Performance Computing

Wen Lee*, Nanxi Li, Hong Cai, Xu Feng, Ting-Ta Chi, Landobasa Y M Tobing, Zhenyu Li, King Jien Chui, Ser Choong Chong, Teck Guan Lim, Lennon Y. T. Lee

Institute of Microelectronics, A*STAR (Agency for Science, Technology and Research), 2 Fusionopolis Way, Singapore 138634, wen_lee@ime.a-star.edu.sg

1. INTRODUCTION

The demands of high-performance computing (HPC) with photonic connected data servers are growing to fulfil heavy computing and data transferring loading requirements. This work aims at creating a photonic engine capable of integration with on-chip laser sources, multiple electronic integrated circuits (EIC), photonic integrated circuits (PIC), fiber array unit (FAU), interposer, and 2.5D HPC chip-on-wafer-on-substrate (CoWoS) package.

2. INTEGRATION METHODOLOGY

To achieve laser integration on 2.5D photonic packaging architecture with efficient coupling to perform low pJ/bit and high bandwidth operation, in this work, a concept for integration of EIC-on-PIC and laser diode (LD)-on-PIC interposer wafer packaging solution is proposed. For LD-on-PIC integration, semiconductor laser is flip-chip bonded on PIC. For EIC-on-PIC integration, a novel sandwich-like 2.5D EIC-on-PIC packaging solution is proposed, as shown in Fig. 1. A process of PIC interposer with double-sided EICs are adopted, which was investigated in [2]. Through-silicon vias (TSVs), micro-bumps

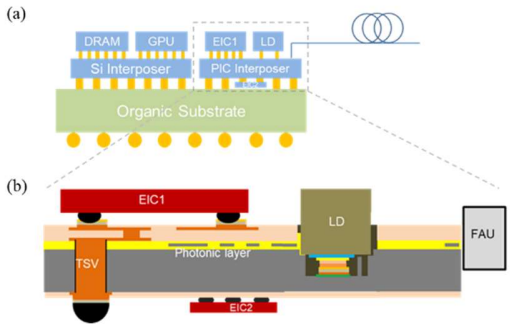

Figure 1 (a) Cross sectional schematic of LD and EIC integrated 2.5D photonic interposer for HPC. (b) Cross sectional schematic of 2.5D LD/EIC-on-PIC interposer photonic engine with fiber array assembly.

and ball grid array (BGA) are used to connect EIC to PIC and EIC to organic substrate. The advantages of this solution are listed as the following. Firstly, all the aggregate interconnects number across the interposer area can increase proportionally with number of channels. Secondly, due to low parasitic and short length of interconnect, it can handle higher data rate. Thirdly, the PIC interposer between LD and EIC can mitigate the electrical and thermal cross talk between them. Therefore, this solution can easily be scaled up to 1.6T data rate and beyond, as the shortest transmission line between PIC interposer, substrate, EICs, and active waveguide modulator enabled in this architecture.

3. DESIGN AND FABRICATION RESULTS

The semiconductor laser is integrated on PIC chip through flip-chip bonding. By using an etch stop layer, the vertical alignment precision can achieve ±50 nm. To further enhance the horizontal alignment tolerance, a multi-tip edge coupler is used for coupling between semiconductor laser and silicon photonics waveguide [1].

A next generation data link photonic engine with coarse wavelength division multiplexing (CWDM) O-band 4λ LD array

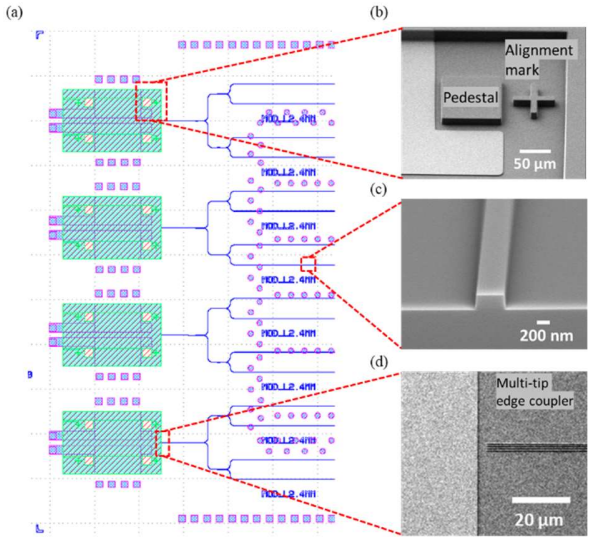

Figure 2 1.6T photonic engine with LD cavity process results. (a) Drawing of photonic engine structure. (b) SEM image of etched cavity for flip-chip laser bonding, including pedestal and alignment mark for LD integration. (c) SEM image of patterned waveguide on PIC. (d) SEM image of multi-tip edge coupler on PIC.

is designed for HPC, with drawing shown in Fig. 2(a). The zoom-in views of fabricated device are also presented in the same figure. The scanning electron microscopy (SEM) image of etched cavity for flip-chip laser bonding is illustrated in Fig. 2(b). The SEM images of patterned waveguide and multi-tip edge coupler on PIC are also included in Fig. 2(c) and 2(d), respectively. Furthermore, preliminary analysis on interconnect performance and RF electrode impedance have been conducted [3].

ACKNOWLEDGMENTS

We acknowledge the funding support from Agency for Science, Technology and Research (A*STAR).

REFERENCES

[1] T. T. Chi et al., “Laser Integration on Silicon through Flip-chip Bonding with Efficient Coupling,” in 2022 IEEE 24th Electronics Packaging Technology Conference (EPTC), Dec. 2022.

[2] P.-J. Tzeng et al., “Process integration of 3D Si interposer with double-sided active chip attachments,” in 2013 IEEE 63rd Electronic Components and Technology Conference, May 2013, pp. 86–93. doi: 10.1109/ECTC.2013.6575555.

[3] F. Xu, T. G. Lim, W. Lee, and L. Zhou, “An EIC on PIC packaging solution for photonic engine of 800G data rate and beyond,” in 2022 IEEE 24th Electronics Packaging Technology Conference (EPTC), Dec. 2022.