PIMID: A Full-System Simulator for Processing-in-Memory with Intricacy and Diversity

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1 INTRODUCTION

Processing-in-Memory (PIM) has emerged as a promising solution to the longstanding memory wall challenge, driven by the increasing disparity between processor and memory performance. As computational demands continue to grow, conventional memory systems struggle to keep pace, prompting the need for innovative approaches that reduce data movement and improve energy efficiency. PIM offers a way forward by integrating computational capabilities directly into memory systems, but current tools for exploring this paradigm remain limited in their scope and flexibility.

To address these shortcomings, we introduce PIMID, a full-system simulation framework tailored for the comprehensive evaluation of PIM architectures. PIMID stands out with its ability to co-simulate host and memory devices in real time, alongside its support for diverse memory technologies. It also allows for detailed and fine-grained configurations of the processing elements (PEs) at various levels plus advanced support for in-memory networks, which enable precise architectural explorations with complex data communication patterns inside the memory. By offering extensive configurability and support for emerging technologies, PIMID serves as a robust foundation for exploring the next generation of memory-centric computing systems.

2 PIMID: DESIGN AND CAPABILITIES

PIMID stands out with its ability to co-simulate host and memory devices in real time with the help of multiple processes of ZSim simulations, alongside its support for diverse memory technologies, including DRAM, SRAM and STT-MRAM. It also allows for detailed and fine-grained configurations of the processing elements (PEs) at various levels, such as subarrays, banks, chips, and stacks, which enable precise architectural explorations.

Another key feature of PIMID is its advanced support for in-memory networks. By integrating detailed network models, it captures complex data communication patterns and addresses often-overlooked challenges, such as disparities in addressing between the host and PEs and the need for realistic interconnect designs.

3 SIMULATION RESULTS

To write [1–6]. To write...

Figure 1: to write.

Figure 2: to write.

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	UPMEM SDK (UPMEM)	**uPIMulator (KAIST)**	**PiMulator (Virginia)**	**ZSim+Ramulator (ETH Zurich)**	**MultiPIM (Virginia)**	**PIMID (RCCS+LANL)**
Simulation or Emulation Model	Functional	Cycle-accurate, extension to UPEMEM SDK	RTL Simulation and FPGA Prototyping	Trace-based	Trace-based, extension to ZSim	Trace-based, extension to MultiPIM and ZSim
Memory Technology Support	DRAM	DRAM	DRAM	DRAM	DRAM	DRAM, SRAM, STT-MRAM
Scope of Simulation and Emulation	PIM Subsystem / Core at Banks	PIM Subsystem / Core at Banks	PIM Subsystem / Core at Banks, Chips, and Ranks	Host and Device, but no co-simulation / Cores at Banks	Host and Device, but no co-simulation / Cores at Banks	Host and Device with co-simulations / Core at Subarrays, Banks, Chips, and Ranks
Network Model	NA	NA	DIY	NA	In-house and BookSim	GARNET
VM Support	NA	NA	DIY	NA	PTW	PTW
Hardware Validation	RDIMM	RDIMM	FPGA	NA	NA	To come

Table 1: Comparisons of Major PIM Research Tools